WHAT IS CLAIMED IS:

1. A semiconductor memory device comprising:

a memory cell having a first transfer MISFET and a second transfer MISFET disposed at portions where a pair of complementary data lines and a word line intersect, a first drive MISFET and a second drive MISFET, and a first vertical MISFET and a second vertical MISFET, the first drive MISFET and the first vertical MISFET, and the second drive MISFET and the second vertical MISFET being cross-connected,

wherein the first and second transfer MISFETs, and the first and second drive MISFETs are formed on a major surface of a semiconductor substrate,

wherein the first and second vertical MISFETs are formed over the first and second transfer MISFETs and the first and second drive MISFETs respectively,

wherein the first vertical MISFET has a source, a channel region and a drain formed in a first laminated body extending in a direction perpendicular to the major surface of the semiconductor substrate, and a gate electrode formed on sidewall portions of the first laminated body with a gate insulating film interposed therebetween,

wherein the second vertical MISFET has a source, a channel region and a drain of a second laminated body extending in a direction perpendicular to the major

surface of the semiconductor substrate, and a gate electrode formed on sidewall portions of the second laminated body with a gate insulating film interposed therebetween, and

wherein the sources of the first and second vertical MISFETs are electrically connected to a source voltage line formed over the first and second laminated bodies.

2. The semiconductor memory device according to claim 1, wherein one of the complementary data lines, which is electrically connected to one of a source and drain of the first transfer MISFET, and the other of the complementary data lines, which is electrically connected to one of a source and drain of the second transfer MISFET, are formed in the same wiring layer as the source voltage line.

3. The semiconductor memory device according to claim 1, wherein the word line electrically connected to gate electrodes of the first and second transfer MISFETs is formed in a wiring layer above the source voltage line and the complementary data lines.

4. The semiconductor memory device according to claim 1, wherein reference voltage lines electrically connected to sources of the first and second drive

MISFETs are formed in the same wiring layer as the word line.

5. The semiconductor memory device according to claim 1, wherein the reference voltage lines comprise a first reference voltage line electrically connected to the source of the first drive MISFET, and a second reference voltage line electrically connected to the source of the second drive MISFET, and the first reference voltage line and the second reference voltage line extend in a first direction with the word line being arranged therebetween.

6. The semiconductor memory device according to claim 5, wherein one of the complementary data lines and the other thereof extend in a second direction intersecting the first direction with the source voltage line being interposed therebetween.

7. The semiconductor memory device according to claim 1, wherein the complementary data lines, the source voltage line, the reference voltage lines and the word line are constituted of a metal film comprised of copper as a principal component.

8. A semiconductor memory device comprising:

a memory cell having a first transfer MISFET and a

second transfer MISFET disposed at portions where a pair of complementary data lines and a word line intersect, a first drive MISFET and a second drive MISFET, and a first vertical MISFET and a second vertical MISFET, the first drive MISFET and the first vertical MISFET, and the second drive MISFET and the second vertical MISFET bing cross-connected,

wherein the first and second transfer MISFETs, and the first and second drive MISFETs are formed on a major surface of a semiconductor substrate,

wherein the first vertical MISFET is disposed on one end of a gate electrode of the second drive MISFET and has a source, a channel region and a drain formed in a first laminated body extending in a direction perpendicular to the major surface of the semiconductor substrate, and a gate electrode formed on sidewall portions of the first laminated body with a gate insulating film interposed therebetween, and

wherein the second vertical MISFET is disposed on one end of a gate electrode of the first drive MISFET and has a source, a channel region and a drain formed in a second laminated body extending in a direction perpendicular to the major surface of the semiconductor substrate, and a gate electrode formed on sidewall portions of the second laminated body with a gate insulating film interposed therebetween.

9. The semiconductor memory device according to claim 8, wherein the first and second vertical MISFETs are disposed between areas for forming the first transfer MISFET and the first drive MISFET and areas for forming the second transfer MISFET and the second drive MISFET as viewed on a plane basis in a plane parallel to the major surface of the semiconductor substrate.

10. A semiconductor memory device comprising:

a memory cell having a first transfer MISFET and a second transfer MISFET disposed at portions where a pair of complementary data lines and a word line intersect, a first drive MISFET and a second drive MISFET, and a first vertical MISFET and a second vertical MISFET, the first drive MISFET and the first vertical MISFET, and the second drive MISFET and the second vertical MISFET being cross-connected,

wherein the first and second transfer MISFETs, and the first and second drive MISFETs are formed on a major surface of a semiconductor substrate,

wherein the first and second vertical MISFETs are formed over the first and second transfer MISFETs and the first and second drive MISFETs,

wherein the first vertical MISFET has a source, a channel region and a drain formed in a first laminated body extending in a direction perpendicular to the major surface of the semiconductor substrate, and a first gate

electrode formed on sidewall portions of the first laminated body with a gate insulating film interposed therebetween,

wherein the second vertical MISFET includes a source, a channel region and a drain formed in a second laminated body extending in a direction perpendicular to the major surface of the semiconductor substrate, and a second gate electrode formed on sidewall portions of the second laminated body with a gate insulating film interposed therebetween,

wherein the drain of the first vertical MISFET, a gate electrode of the second drive MISFET, and a drain of the first drive MISFET are electrically connected to one another through a first intermediate conductive layer,

wherein the drain of the second vertical MISFET, a gate electrode of the first drive MISFET, and a drain of the second drive MISFET are electrically connected to one another through a second intermediate conductive layer,

wherein the first gate electrode of the first vertical MISFET is electrically connected to the second intermediate conductive layer through a first gate drawing electrode formed so as to come into contact with the first gate electrode, and a first conductive layer lying in a first connecting hole and formed so as to come into contact with the first gate drawing electrode and the second intermediate conductive layer, and

wherein the second gate electrode of the second

vertical MISFET is electrically connected to the first intermediate conductive layer through a second gate drawing electrode formed so as to come into contact with the second gate electrode, and a second conductive layer lying in a second connecting hole and formed so as to come into contact with the second gate drawing electrode and the first intermediate conductive layer.

11. The semiconductor memory device according to claim 10, wherein a plurality of MISFETs for each peripheral circuit are further formed on the major surface of the semiconductor substrate, and wirings for connecting between the MISFETs of the peripheral circuit and the first and second intermediate conductive layers are formed in the same wiring layer.

12. The semiconductor memory device according to claim 10, wherein the first and second intermediate conductive layers are comprised of a metal film, a first barrier layer is formed between the drain of the first vertical MISFET and the first intermediate conductive layer, and a second barrier layer is formed between the drain of the second vertical MISFET and the second intermediate conductive layer.

13. The semiconductor memory device according to claim 12, wherein the first and second intermediate

conductive layers are constituted of a tungsten film, and the first and second barrier layers comprise a tungsten nitride (WN) film.

14. The semiconductor memory device according to claim 10, wherein the first and second intermediate conductive layers are constituted of an oxidation resistant conductive film.

15. The semiconductor memory device according to claim 10, wherein the first gate electrode of the first vertical MISFET is electrically connected to the first gate drawing electrode at a lower end thereof, and the second gate electrode of the second vertical MISFET is electrically connected to the second gate drawing electrode at a lower end thereof.

16. The semiconductor memory device according to claim 10, wherein the first gate electrode of the first vertical MISFET and the second gate electrode of the second vertical MISFET are respectively comprised of two-layer conductive films.

17. The semiconductor memory device according to claim 10, wherein the second intermediate conductive layer, the first gate drawing electrode and the first connecting hole are disposed so as to have portions which

overlap each other on a plane basis, whereas the first intermediate conductive layer, the second gate drawing electrode and the second connecting hole are disposed so as to have portions which overlap each other on a plane basis.

18. The semiconductor memory device according to claim 10, wherein the first connecting hole extends through the first gate drawing electrode to connect to the second intermediate conductive layer, and the second connecting hole extends through the second gate drawing electrode to connect to the first intermediate conductive layer.

19. The semiconductor memory device according to claim 10, wherein the first gate drawing electrode is brought into contact with the first gate electrode of the first vertical MISFET at the sidewall portions of the first laminated body, and the second gate drawing electrode is brought into contact with the second gate electrode of the second vertical MISFET at the sidewall portions of the second laminated body.

20. The semiconductor memory device according to claim 10, wherein the first gate drawing electrode is formed integrally with the first gate electrode of the first vertical MISFET, and the second gate drawing

electrode is formed integrally with the second gate electrode of the second vertical MISFET.

21. The semiconductor memory device according to claim 10, wherein the gate electrode of the first vertical MISFET is formed so as to surround the sidewall portions of the first laminated body, and the gate electrode of the second vertical MISFET is formed so as to surround the sidewall portions of the second laminated body.

22. The semiconductor memory device according to claim 10, wherein each of the first and second gate drawing electrodes is comprised of a silicon conductive film and a silicide film formed on the surface thereof.

23. The semiconductor memory device according to claim 1, wherein the first and second transfer MISFETs, and the first and second drive MISFETs comprise n channel type MISFETs respectively, and the first and second vertical MISFETs comprise p channel type MISFETs respectively.

24. A method of manufacturing a semiconductor memory device comprising a memory cell which includes a first transfer MISFET and a second transfer MISFET disposed at portions where a pair of complementary data

lines and a word line intersect, a first drive MISFET and a second drive MISFET, and a first vertical MISFET and a second vertical MISFET, the first drive MISFET and the first vertical MISFET, and the second drive MISFET and the second vertical MISFET being cross-connected,

wherein the first vertical MISFET has a source, a channel region and a drain formed in a first laminated body extending in a direction perpendicular to a major surface of a semiconductor substrate, and a gate electrode formed on sidewall portions of the first laminated body with a gate insulating film interposed therebetween, and

wherein the second vertical MISFET has a source, a channel region and a drain formed in a second laminated body extending in a direction perpendicular to the major surface of the semiconductor substrate, and a gate electrode formed on sidewall portions of the second laminated body with a gate insulating film interposed therebetween, said method comprising the steps of:

(a) forming the first and second transfer MISFETs and first and second drive MISFETs in a first area of the major surface of the semiconductor substrate;

(b) forming a first intermediate conductive layer for electrically connecting a gate electrode of the second drive MISFET with a drain of the first drive MISFET over the first and second transfer MISFETs and the first and second drive MISFETs, and forming a second

intermediate conductive layer for electrically connecting a gate electrode of the first drive MISFET with a drain of the second drive MISFET over the first and second transfer MISFETs and the first and second drive MISFETs;

(c) forming first and second gate drawing electrodes over the first and second intermediate conductive layers with a first insulating film interposed therebetween;

(d) after the step (c), forming the first and second laminated bodies over the first and second gate drawing electrodes to thereby electrically connect a drain of a first vertical MISFET formed in the first laminated body with the first intermediate conductive layer and electrically connect a drain of a second vertical MISFET formed in the second laminated body with the second intermediate conductive layer;

(e) electrically connecting a gate electrode of the first vertical MISFET, which is formed on sidewall portions of the first laminated body with a gate insulating film interposed therebetween, with the first gate drawing electrode, and electrically connecting a gate electrode of the second vertical MISFET, which is formed on sidewall portions of the second laminated body with a gate insulating film interposed therebetween, with the second gate drawing electrode; and

(f) forming a first connecting hole over the first gate drawing electrode so as to come into contact with

the first gate drawing electrode and the second intermediate conductive layer and embedding a first conductive layer into the first connecting hole, and forming a second connecting hole over the second gate drawing electrode so as to come into contact with the second gate drawing electrode and the first intermediate conductive layer and embedding a second conductive layer into the second connecting hole.

25. The method according to claim 24,

wherein the step (c) includes sub-steps of: forming a barrier layer on the surfaces of the first and second intermediate conductive layers; and forming the first and second gate drawing electrodes over the first and second intermediate conductive layers formed with the barrier layer with the first insulating film interposed therebetween,

wherein the step (d) includes sub-steps of: forming a second insulating film for covering the first insulating film and the first and second gate drawing electrodes; etching the second insulating film and the first insulating film to thereby form a first opening for exposing the barrier layer on the surface of the first intermediate conductive layer and a second opening for exposing the barrier layer on the surface of the second intermediate conductive layer; embedding a conductive layer into the first and second openings; and forming the

first and second laminated bodies over the second insulating film to thereby electrically connect the drain of the first vertical MISFET formed in the first laminated body with the first intermediate conductive layer through the barrier layer and the conductive layer lying inside the first opening, and electrically connect the drain of the second vertical MISFET formed in the second laminated body with the second intermediate conductive layer through the barrier layer and the conductive layer lying inside the second opening,

wherein the step (e) includes sub-steps of: annealing the semiconductor substrate in a state in which the first and second gate drawing electrodes and the conductive film lying inside the first and second openings are being covered with the second insulating film, to thereby form the gate insulating film on each of the sidewall portions of the first and second laminated bodies; etching a first gate electrode material deposited on the semiconductor substrate to thereby form a first gate electrode layer on the sidewall portions of the first and second laminated bodies; etching the second insulating film to thereby expose the first and second gate drawing electrodes; and etching a second gate electrode material deposited on the semiconductor substrate to thereby form a second gate electrode layer on the sidewall portions of the first and second laminated bodies, which are formed with the first gate

electrode layer, and electrically connecting the second gate electrode layer formed on the sidewall portions of the first laminated body with the first gate drawing electrode, and electrically connecting the second gate electrode layer formed on the sidewall portions of the first laminated body with the first gate drawing electrode.

26. A method of manufacturing a semiconductor memory device comprising a memory cell which includes a first transfer MISFET and a second transfer MISFET disposed at portions where a pair of complementary data lines and a word line intersect, a first drive MISFET and a second drive MISFET, and a first vertical MISFET and a second vertical MISFET, the first drive MISFET and the first vertical MISFET, and the second drive MISFET and the second vertical MISFET being cross-connected,

wherein the first vertical MISFET has a source, a channel region and a drain formed in a first laminated body extending in a direction perpendicular to a major surface of a semiconductor substrate, and a gate electrode formed on sidewall portions of the first laminated body with a gate insulating film interposed therebetween, and

wherein the second vertical MISFET has a source, a channel region and a drain formed in a second laminated body extending in a direction perpendicular to the major

surface of the semiconductor substrate, and a gate electrode formed on sidewall portions of the second laminated body with a gate insulating film interposed therebetween, said method comprising the steps of:

(a) forming the first and second transfer MISFETs and first and second drive MISFETs in a first area of the major surface of the semiconductor substrate;

(b) forming a first intermediate conductive layer for electrically connecting a gate electrode of the second drive MISFET with a drain of the first drive MISFET over the first and second transfer MISFETs and the first and second drive MISFETs, and forming a second intermediate conductive layer for electrically connecting a gate electrode of the first drive MISFET with a drain of the second drive MISFET over the first and second transfer MISFETs and the first and second drive MISFETs;

(c) after the step (b), forming first and second laminated bodies over the first and second intermediate conductive layers to thereby electrically connect a drain of a first vertical MISFET formed in the first laminated body with the first intermediate conductive layer and electrically connect a drain of a second vertical MISFET formed in the second laminated body with the second intermediate conductive layer;

(d) after the step (c), forming a first gate drawing electrode so as to come into contact with a gate electrode of the first vertical MISFET, which is formed

on sidewall portions of the first laminated body with a gate insulating film therebetween, and forming a second gate drawing electrode so as to come into contact with a gate electrode of the second vertical MISFET, which is formed on sidewall portions of the second laminated body with a gate insulating film interposed therebetween; and

(e) forming a first connecting hole over the first gate drawing electrode so as to come into contact with the first gate drawing electrode and the second intermediate conductive layer and embedding a first conductive layer into the first connecting hole, and forming a second connecting hole over the second gate drawing electrode so as to come into contact with the second gate drawing electrode and the first intermediate conductive layer and embedding a second conductive layer into the second connecting hole.

27. The method according to claim 24, further including a step of forming a source voltage line electrically connected to the sources of the first and second vertical MISFETs over the first and second laminated bodies after the step (e).

28. The method according to claim 27, further including a step of forming one of the complementary data lines, which is electrically connected to one of a source and drain of the first transfer MISFET, and the other

thereof electrically connected to one of a source and drain of the second transfer MISFET in the source voltage line forming step.

29. The method according to claim 27, further including a step of forming the word line electrically connected to gate electrodes of the first and second transfer MISFETs and reference voltage lines electrically connected to sources of the first and second drive MISFETs over the source voltage line.

30. A semiconductor memory device comprising:

a memory cell provided with a first drive MISFET and a second drive MISFET and a first vertical MISFET and a second vertical MISFET,

wherein the drive MISFETs are formed on a major surface of a semiconductor substrate,

wherein a metal film is formed over the drive MISFETs with an insulating film interposed therebetween, and

wherein the vertical MISFETs are formed over the metal film.

31. A semiconductor memory device comprising:

a memory cell which includes a first drive MISFET and a second drive MISFET and a first vertical MISFET and a second vertical MISFET, the first drive MISFET and the

first vertical MISFET, and the second drive MISFET and the second vertical MISFET being cross-connected,

wherein the drive MISFETs are formed on a major surface of a semiconductor substrate,

wherein a metal film for cross-connecting gates and drains of the first and second drive MISFETs is formed over the drive MISFETs with an insulating film interposed therebetween, and

wherein the vertical MISFETs connected to the metal film are formed over the metal film.

32. The semiconductor memory device according to claim 30, wherein the metal film includes a tungsten film, and the first and second vertical MISFETs and the tungsten film are respectively electrically connected via a barrier film.

33. A semiconductor memory device comprising:

a memory cell which includes a first drive MISFET and a second drive MISFET and a first vertical MISFET and a second vertical MISFET, the first drive MISFET and the first vertical MISFET, and the second drive MISFET and the second vertical MISFET being cross-connected,

wherein the drive MISFETs are formed on a major surface of a semiconductor substrate, and

wherein gates of the vertical MISFETs formed over the drive MISFETs with an insulating film interposed

therebetween are electrically connected to lower conductive films at lower portions thereof and thereby electrically connected to gates or drains of the drive MISFETs.

34. A semiconductor memory device comprising:

a memory cell which includes a first drive MISFET and a second drive MISFET and a first vertical MISFET and a second vertical MISFET, the first drive MISFET and the first vertical MISFET, and the second drive MISFET and the second vertical MISFET being cross-connected,

wherein the drive MISFETs are formed on a major surface of a semiconductor substrate,

wherein the vertical MISFETs are respectively formed over the drive MISFETs with an insulating film interposed therebetween, and

wherein current paths between gates or drains of the drive MISFETs and gates of the vertical MISFETs are formed via lower portions of the gates of the vertical MISFETs through conductive films.

35. A semiconductor memory device comprising:

a memory cell which includes a first drive MISFET and a second drive MISFET and a first vertical MISFET and a second vertical MISFET, the first drive MISFET and the first vertical MISFET, and the second drive MISFET and the second vertical MISFET being cross-connected,

wherein the drive MISFETs are formed on a major surface of a semiconductor substrate,

wherein conductive films electrically connected to gates or drains of the drive MISFETs are respectively formed over the drive MISFETs with an insulating film interposed therebetween,

wherein the vertical MISFETs are formed over the conductive films, and

wherein gate electrodes of the vertical MISFETs are shaped in the form of sidewall spacers and electrically connected to the conductive films.

36. A semiconductor memory device comprising:

a memory cell which includes a first drive MISFET and a second drive MISFET and a first vertical MISFET and a second vertical MISFET, the first drive MISFET and the first vertical MISFET, and the second drive MISFET and the second vertical MISFET being cross-connected,

wherein the drive MISFETs are formed on a major surface of a semiconductor substrate,

wherein conductive films electrically connected to gate electrodes or drains of the drive MISFETs are formed over the drive MISFETs with an insulating film interposed therebetween,

wherein the vertical MISFETs are formed over the conductive films, and

wherein gate electrodes of the vertical MISFETs are

electrically connected to the conductive films in a self-alignment manner.

37. The semiconductor memory device according to claim 33,

wherein the vertical MISFETs are formed over the conductive films with an insulating film interposed therebetween,

wherein the gate electrodes of the vertical MISFETs respectively include a first film and a second film shaped in the form of sidewall spacers,

wherein the conductive film is opened in a self-alignment with the first film, and

wherein the second film is electrically connected to the corresponding conductive film.

38. A semiconductor memory device comprising:

a memory cell which includes a first drive MISFET and a second drive MISFET and a first vertical MISFET and a second vertical MISFET, the first drive MISFET and the first vertical MISFET, and the second drive MISFET and the second vertical MISFET being cross-connected,

wherein the drive MISFETs are formed on a major surface of a semiconductor substrate,

wherein a first conductive film electrically connected to a gate or drain of each of the drive MISFETs is formed over the corresponding drive MISFET with an

insulating film interposed therebetween,

wherein a second conductive film is formed over the first conductive film,

wherein each of the vertical MISFETs is formed over the second conductive film,

wherein a gate of the corresponding vertical MISFET is electrically connected to the second conductive film, and

wherein a drain of the corresponding vertical MISFET is electrically connected to the first conductive film not through the second conductive film.

39. The semiconductor memory device according to claim 38,

wherein each of the vertical MISFETs is formed over the second conductive film with an insulating film interposed therebetween,

wherein the gates of the vertical MISFETs respectively include a first film and a second film shaped in the form of sidewall spacers,

wherein the second conductive film is opened in a self-alignment with the first film, and

wherein the second film is electrically connected to the second conductive film.

40. The semiconductor memory device according to claim 38,

wherein the first conductive film is comprised of a metal film,

wherein the second conductive film is comprised of a silicon film, and

wherein the first conductive film is electrically connected to the drain of each of the vertical MISFETs via a barrier film.

41. The semiconductor memory device according to claim 38, wherein conductive films, which are conductive films lying in the same layer as the first conductive film for electrical connection between gates and drains of MISFETs for each peripheral circuit, are formed.

42. A semiconductor memory device comprising:

a memory cell having a first drive MISFET and a second drive MISFET and a first vertical MISFET and a second vertical MISFET; and

MISFETs for a peripheral circuit,

wherein the drive MISFETs are formed on a major surface of a semiconductor substrate,

wherein conductive films for electrical connection between gates and drains of the drive MISFETs, are formed over the drive MISFETs with an insulating film interposed therebetween,

wherein the vertical MISFETs are formed over the conductive films, and

wherein conductive films, which are conductive films lying in the same layer as said conductive films and carry out electrical connection between gates and drains of the MISFETs for the peripheral circuit, are formed.

43. The semiconductor memory device according to claim 42,

wherein the conductive films are respectively constituted of a metal film, and

wherein the conductive films are electrically connected to drains of the vertical MISFETs via barrier films.

44. The semiconductor memory device according to claim 42,

wherein a metal wiring layer is formed through an insulating film which covers the vertical MISFETs, and

wherein wirings for electrical connection between the gates and drains of the MISFETs for the peripheral circuit are formed by the metal wiring layer.

45. A semiconductor memory device comprising:

a memory cell having a first drive MISFET and a second drive MISFET and a first vertical MISFET and a second vertical MISFET,

wherein the drive MISFETs are formed on a major

surface of a semiconductor substrate,

wherein conductive films electrically connected to gates or drains of the drive MISFETs are formed over the drive MISFETs with an insulating film interposed therebetween,

wherein the vertical MISFETs are formed over the conductive films, and

wherein the conductive films and gate electrodes of the vertical MISFETs are respectively electrically connected by plugs embedded in connecting holes formed in an insulating film covering the vertical MISFETs.

46. The semiconductor memory device according to claim 45, wherein conductive films, which are conductive films lying in the same layer as said conductive films for electrical connection between gates and drains of MISFETs for a peripheral circuit, are formed.

47. The semiconductor memory device according to claim 30,

wherein each of the vertical MISFETs has a source, a channel region and a drain formed in a laminated body extending in a direction perpendicular to the major surface of the semiconductor substrate, and a gate electrode formed on sidewall portions of the laminated body with a gate insulating film interposed therebetween, and

wherein the laminated body is comprised of a silicon film.

48. A method of manufacturing a semiconductor memory device having a memory cell provided with a first drive MISFET and a second drive MISFET and a first vertical MISFET and a second vertical MISFET, comprising the steps of:

forming drive MISFETs on a major surface of a semiconductor substrate;

forming conductive films electrically connected to gates or drains of the drive MISFETs over the drive MISFETs with an insulating film interposed therebetween;

forming vertical MISFETs over the conductive films;

forming connecting holes in an insulating film which covers the vertical MISFETs; and

embedding plugs into the connecting holes to thereby electrically connect the conductive films with gate electrodes of the vertical MISFETs within the connecting holes respectively.

49. The method according to claim 48, wherein conductive films are formed which are conductive films lying in the same layer as the conductive films for electrical connection between gates and drains of MISFETs for a peripheral circuit.

50. A method of manufacturing a semiconductor memory device having a memory cell provided with a first drive MISFET and a second drive MISFET and a first vertical MISFET and a second vertical MISFET, comprising the steps of:

forming drive MISFETs on a major surface of a semiconductor substrate;

forming semiconductor films each used as a drain/channel/source and a cap insulating film over the drive MISFETs with insulating films interposed therebetween;

patterning the semiconductor films and cap insulating film into columnar shapes;

forming an etching stopper film on side walls of each columnar cap insulating film in side spacer form;

forming an interlayer insulating film on the cap insulating film and etching stopper film; and

etching the interlayer insulating film and cap insulating film, using the etching stopper film as a stopper and thereafter etching the etching stopper film to thereby form connecting holes for opening the semiconductor film.

51. The semiconductor memory device according to claim 10, wherein the first and second gate drawing electrodes are respectively comprised of a metal nitride film.

52. The semiconductor memory device according to claim 16, wherein the first and second gate drawing electrodes are respectively comprised of a metal nitride film, and the conductive film brought into contact with the first gate drawing electrode, of the two-layer conductive films constituting the first gate electrode of the first vertical MISFET, and the conductive film brought into contact with the second gate drawing electrode, of the two-layer conductive films constituting the second gate electrode of the second vertical MISFET are respectively comprised of a metal film.

53. The semiconductor memory device according to claim 12,

wherein the drain of the first vertical MISFET is electrically connected to the first barrier layer through a first plug formed of a silicon film,

wherein the drain of the second vertical MISFET is electrically connected to the second barrier layer through a second plug formed of a silicon film,

wherein a first reactive layer for preventing a reaction between the first plug and the first barrier layer is formed therebetween, and

wherein a second reactive layer for preventing a reaction between the second plug and the second barrier layer is formed therebetween.

54. The semiconductor memory device according to claim 53, wherein depressions and projections are provided on the surfaces of the first and second reactive layers.

55. The semiconductor memory device according to claim 53, wherein the silicon film constituting each of the first and second plugs is one formed by annealing an amorphous silicon film deposited by a CVD method using a source gas containing disilane.

56. A method of manufacturing a semiconductor memory device comprising a memory cell which includes a first transfer MISFET and a second transfer MISFET disposed at portions where a pair of complementary data lines and a word line intersect, a first drive MISFET and a second drive MISFET, and a first vertical MISFET and a second vertical MISFET, the first drive MISFET and the first vertical MISFET, and the second drive MISFET and the second vertical MISFET being cross-connected,

wherein the first vertical MISFET has a source, a channel region and a drain formed in a first laminated body extending in a direction perpendicular to a major surface of a semiconductor substrate, and a first gate electrode formed on sidewall portions of the first laminated body with a gate insulating film interposed

therebetween, and

wherein the second vertical MISFET has a source, a channel region and a drain formed in a second laminated body extending in a direction perpendicular to the major surface of the semiconductor substrate, and a second gate electrode formed on sidewall portions of the second laminated body with a gate insulating film interposed therebetween,

said method comprising a step of forming the first gate electrode of the first vertical MISFET and the second gate electrode of the second vertical MISFET,

said step including sub-steps of:

(a) depositing an amorphous silicon film on the semiconductor substrate and anisotropically etching the amorphous silicon film to thereby form a sidewall spacer-shaped amorphous silicon layer on each of the sidewall portions of the first and second laminated bodies;

(b) after the step (a), depositing a polycrystal silicon film on the semiconductor substrate and anisotropically etching the polycrystal silicon film to thereby form a sidewall spacer-shaped polycrystal silicon layer on the surface of the amorphous silicon layer formed on each of the sidewall portions of the first and second laminated bodies; and

(c) polycrystallizing the amorphous silicon layer by annealing.

57. A method of manufacturing a semiconductor memory device comprising a memory cell which includes a first transfer MISFET and a second transfer MISFET disposed at portions where a pair of complementary data lines and a word line intersect, a first drive MISFET and a second drive MISFET, and a first vertical MISFET and a second vertical MISFET, the first drive MISFET and the first vertical MISFET, and the second drive MISFET and the second vertical MISFET being cross-connected,

wherein the first vertical MISFET has a source, a channel region and a drain formed in a first laminated body extending in a direction perpendicular to a major surface of a semiconductor substrate, and a gate electrode formed on sidewall portions of the first laminated body with a gate insulating film interposed therebetween, and

wherein the second vertical MISFET has a source, a channel region and a drain formed in a second laminated body extending in a direction perpendicular to the major surface of the semiconductor substrate, and a gate electrode formed on sidewall portions of the second laminated body with a gate insulating film interposed therebetween,

said method comprising a step of forming gate electrodes of the first and second transfer MISFETs and gate electrodes of the first and second drive MISFETs,

said step including:

(a) a step of forming a mask layer over a first conductive film constituting each of the gate electrodes of the first and second transfer MISFETs and each of the gate electrodes of the first and second drive MISFETs;

(b) a first step of patterning the mask layer along a first direction of the major surface of the semiconductor substrate;

(c) a second step of patterning the mask layer along a second direction intersecting the first direction; and

(d) a step of patterning the first conductive film with the mask layer as a mask after the step (c).

58. A method of manufacturing a semiconductor memory device comprising a memory cell which includes a first transfer MISFET and a second transfer MISFET disposed at portions where a pair of complementary data lines and a word line intersect, a first drive MISFET and a second drive MISFET, and a first vertical MISFET and a second vertical MISFET, the first drive MISFET and the first vertical MISFET, and the second drive MISFET and the second vertical MISFET being cross-connected,

wherein the first vertical MISFET has a source, a channel region and a drain formed in a first laminated body extending in a direction perpendicular to a major surface of a semiconductor substrate, and a gate electrode formed on sidewall portions of the first

laminated body with a gate insulating film interposed therebetween, and

wherein the second vertical MISFET has a source, a channel region and a drain formed in a second laminated body extending in a direction perpendicular to the major surface of the semiconductor substrate, and a gate electrode formed on sidewall portions of the second laminated body with a gate insulating film interposed therebetween,

said method comprising a step of forming channel regions of the first and second vertical MISFETs,

said step including sub-steps of:

(a) depositing an amorphous silicon film over a conductive film constituting each of the sources of the first and second vertical MISFETs by a CVD method using disilane as a source gas; and

(b) polycrystallizing the amorphous silicon film by annealing.

59. A method of manufacturing vertical MISFETs each having a source, a channel region and a drain formed in at least one laminated body extending in a direction perpendicular to a major surface of a semiconductor substrate, and a gate electrode formed on sidewall portions of the laminated body with a gate insulating film interposed therebetween,

said method comprising a step of forming the gate

electrode,

said step including sub-steps of:

(a) depositing an amorphous silicon film on a semiconductor substrate and anisotropically etching the amorphous silicon film to thereby form a sidewall spacer-shaped amorphous silicon layer on the sidewall portions of the laminated body;

(b) after the step (a), depositing a polycrystal silicon film on the semiconductor substrate and anisotropically etching the polycrystal silicon film to thereby form a sidewall spacer-shaped polycrystal silicon layer on the surface of the amorphous silicon layer formed on the sidewall portions of the laminated body; and

(c) polycrystallizing the amorphous silicon layer by annealing.

60. A method of manufacturing a semiconductor device comprising:

(a) a step of forming a mask layer over a first conductive film constituting a gate electrode of a first MISFET and a gate electrode of a second drive MISFET;

(b) a first step of patterning the mask layer along a first direction of a major surface of a semiconductor substrate;

(c) a second step of patterning the mask layer along a second direction intersecting the first

direction; and

(d) a step of patterning the first conductive film with the mask layer as a mask after the step (c).

61. A method of manufacturing vertical MISFETs each having a source, a channel region and a drain formed in a laminated body extending in a direction perpendicular to a major surface of a semiconductor substrate, and a gate electrode formed on sidewall portions of the laminated body with a gate insulating film interposed therebetween,

said method comprising a step of forming channel regions of the first and second vertical MISFETs,

said step including sub-steps of:

(a) depositing an amorphous silicon film over a conductive film constituting each of the sources of the first and second vertical MISFETs by a CVD method using disilane as a source gas; and

(b) polycrystallizing the amorphous silicon film by annealing.

62. A vertical MISFET comprising:

a source, a channel region and a drain formed in a laminated body extending in a direction perpendicular to a major surface of a semiconductor substrate, and a gate electrode formed on sidewall portions of the laminated body with a gate insulating film interposed therebetween,

wherein a gate of the vertical MISFET includes a

first film formed in sidewall spacer form on a self-alignment basis with respect to the laminated body, and a second film formed in sidewall spacer form in a self-alignment with the first film.

63. A semiconductor device comprising:

MISFETs; and

vertical MISFETs,

wherein the MISFETs are formed on a major surface of a semiconductor substrate, a metal film is formed over said each MISFET with an insulating film interposed therebetween, and the vertical MISFETs are formed over the metal film.

64. A semiconductor device comprising:

MISFETs; and

vertical MISFETs,

wherein the MISFETs are formed on a major surface of a semiconductor substrate, and

wherein gates of the vertical MISFETs formed over the MISFETs with an insulating film interposed therebetween are respectively electrically connected to lower conductive films at lower portions thereof and thereby electrically connected to gates or drains of the MISFETs.

65. A semiconductor device comprising:

MISFETs; and

vertical MISFETs,

wherein the MISFETs are formed on a major surface of a semiconductor substrate,

wherein each of the vertical MISFETs is formed over said each MISFET with an insulating film interposed therebetween, and

wherein current paths between gates or drains of the MISFETs and gates of the vertical MISFETs are respectively formed via lower portions of the gates of the vertical MISFETs through conductive films.

66. A semiconductor device comprising:

MISFETs; and

vertical MISFETs,

wherein the MISFETs are formed on a major surface of a semiconductor substrate,

wherein conductive films electrically connected to gates or drains of the MISFETs are respectively formed over the MISFETs with insulating films interposed therebetween,

wherein the vertical MISFETs are formed over the conductive films, and

wherein gates of the vertical MISFETs are respectively shaped in the form of sidewall spacers and electrically connected to the conductive films.

67. A semiconductor device comprising:

MISFETs; and

vertical MISFETs,

wherein the MISFETs are formed on a major surface of a semiconductor substrate,

wherein conductive films electrically connected to gates or drains of the MISFETs are respectively formed over the MISFETs with insulating films interposed therebetween,

wherein the vertical MISFETs are formed over the conductive films, and

wherein gates of the vertical MISFETs are respectively electrically connected to the conductive films in a self-alignment manner.

68. A semiconductor device comprising:

a first circuit having a first MISFET and a vertical MISFET; and

a second circuit having a second MISFET,

wherein the first MISFET is formed on a major surface of a semiconductor substrate,

wherein a conductive film for electrical connection between a gate and drain of the first MISFET, is formed over the first MISFET with an insulating film interposed therebetween,

wherein the vertical MISFET is formed over the conductive film, and

wherein a conductive film, which is a conductive film lying in the same layer as the conductive film for electrical connection between a gate and drain of the second MISFET, is formed.